Replacement Paragraphs

Page 4, Paragraph 3:

So, with the source and body grounded, the drain biased at some positive voltage (5.0 volts, for example), and the control gate biased greater than the threshold voltage (2.5 volts, for example), the NMOS transistor in an unprogrammed EPROM in the "on" state and drain current flows.

Page 5, Paragraph 1:

To program the EPROM, the bias conditions are set momentarily so that there is a substantial amount of drain current flowing and hot electrons are generated. Typical bias conditions might be 7.0 volts on the drain and 12.0 volts on the control gate. With these bias conditions, a tremendous amount of hot electrons are generated in a typical 5V, 0.5 micron NMOS transistor. With 12.0 volts on the control gate, there might be 10.0 volts or more across the NMOS gate oxide according to the equation given above. This gate oxide potential "assists" the injection of hot electrons (which already have an abundance of energy) through the gate oxide onto the polysilicon gate. Since the polysilicon gate is a floating gate without connections, these electrons are trapped here due to the oxide insulators which encapsulate the polysilicon once the programming event is completed. After ~200 milliseconds (a typical duration of the programming event), the amount of electrons trapped on the floating gate is significant and sufficient to drastically impact the NMOS transistor characteristics. During such programming, it is possible to increase the NMOS transistor threshold voltage to 4.0-10.0 volts. Assuming this new, higher threshold voltage and the same operating bias conditions described above (5.0 volts on the drain and 2.5 volts on the control gate), the NMOS transistor of the EPROM is now in the "off" state (negligible drain current flowing). By selectively programming EPROMs on a circuit depending on the circuit behavior, the circuit can be trimmed or fine-tuned to enhance its performance. It should be noted at this time that 200 milliseconds to program a single EPROM can be very costly. On a complex

circuit, it is possible that several programming iterations must be performed for each circuit which can significantly added to the probe/test cost. A faster programming EPROM could reduce probe/test cost significantly.

Page 9, Paragraph 2:

Referring to Figure 4, there is illustrated a top down view of an NMOS transistor 101 suitable for use as an EPROM cell according to the invention. The NMOS transistor 101 includes a drain 2 and a source 3 of a N^+ regions 4 and 14. Additionally, there is a poly gate 1 with a P well 6 located beneath the poly gate 1 and the N^+ regions 4 and 14. Lightly doped drain (Nldd) regions 5 and 15 are located beneath the N^+ regions 4 and 14 and extends into the channel region under the poly gate 1. Oxide spacers 7 and 17 are located on the top surface of the substrate adjacent to the poly gate 1 and are used during the implanting of the N^+ region 4 and 14 as a masked for the drain 2 and source 3. Novel P regions 8 and 18 are located beneath the poly gate 1 and separated from the N^+ regions 4 and 14 by the Nldd regions 5 and 15, respectively. The P regions 8 and 18 extend into the P well 6 from the outer periphery 51 but are not present in the center 50 of the NMOS transistor 101. In a pure CMOS process flow, the new P regions 8 and 18 and the P well 6 are positioned prior to the poly gate 1 formation.

Page 9, Paragraph 3:

The P regions 8 and 18 may or may not be completely counter dope to the Nldd region 5 and 15 and may or may not actually intersect with the N^+ regions 4 and 14. The purpose of the P regions 8 and 18 is to increase the electric field between the N^+ region 4 and P well 6. This increase in the electric field will increase the hot electron generation rate in programming an EPROM cell and thus will enable the NMOS transistor 101 to be programmed quicker and possibly at a lower voltage than the prior art devices.